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*(Use as many sheets as necessary)*

Sheet 1 of 1

| *Complete if Known* | |
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| Application Number | 09/808,864 |
| Filing Date | March 15, 2001 |
| First Named Inventor | Jigish D. Trivedi |
| Art Unit | 2823 |
| Examiner Name | George R. Fourson III |
| Attorney Docket Number | MIO 0079 PA/40509.148 |

## NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
|---|---|---|---|
| GF | | TSUKAMOTO et al.; 0.25um W-Polycide Dual Gate and Buried Metal on Diffusion Layer (BMD) Technology for DRAM-Embedded Logic Devices; Symposium on VLSI Technology Digest of Technical Papers; 1997; pp. 23-24; System LSI Division, Semiconductor Company, SONY | |
| | | Corporation, Japan | |
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| Examiner Signature | FOURSON | Date Considered | 7/8/04 |
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